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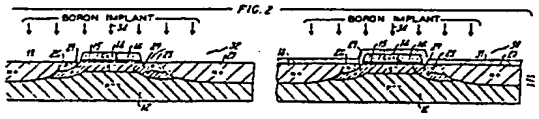
(54) Method of late programming a read only memory.

(57) Transistors (10) having lateral gaps between their source and drain and the gate are interconnected in a ROM to receive program code.

In one embodiment of the invention (Fig. 3), the gaps of selected transistors (42) are subjected to a phosphorous implant (44) to create lightly doped n- regions (26.28) connecting the source (18) and drain (20) to the gate (14), and function normally. The other transistors (40) do not receive the phosphorous implant, and thus have a higher threshold voltage.

In another embodiment of the invention (Fig. 2) all of the transistors receive the phosphorous implant to create the n- regions (26.28) connecting the source and drain to the gate, and the n- regions of selected transistors (32) are counter-doped with a boron implant (34) so as to raise their threshold voltages, while the other transistors (30) are not counter-doped and function normally.

In both embodiments, programming can occur late in the processing of the ROM.



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EUROPEAN SEARCH REPORT

Application number

EP 86 40 1508

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
Y,D	EP-A-0 083 447 (MOSTEK) * Figure 7; page 8, line 1 - page 11, line 9 *	1-3	H 01 L 21/82 H 01 L 27/10
Y	EP-A-0 112 983 (IBM) * Figure 4; page 11, line 28 - page 12, line 31 *	1-3	
Y	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 15, no. 9, February 1973, pages 2919-2920, New York, US; R.W. KNEPPER: "FET array personalization by ion implantation" * Whole document *	1-3	
X	Idem	4	TECHNICAL FIELDS SEARCHED (Int. Cl.4)
			H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	02-04-1987	MACHEK, J.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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Method of Late Progamming a Read Only Memory

Cross Reference to Related Applications

Cross reference is made herein to copending, commonly-owned U.S. Patent Application Serial No. 335,608, entitled TRIPLE DIFFUSED SHORT CHANNEL DEVICE STRUCTURE, filed on even date herewith by Y. P. Han and T. C. Chan.

Technical Field of the Invention

The invention relates to the manufacture and programming of semiconductor Read Only Memories (ROM'S).

Background of the Invention

For faster turnaround of ROM's, there is a need to program them as late in the fabrication sequence as possible, so that few (if any) process steps separate the unprogrammed chip from shipment.

Generally, two types of late programming are employed, post-poly (polycrystalline silicon) and post-metal. Both techniques usually rely on high-energy ion implantation, of boron for example, to increase the boron doping concentration in the channel region beneath the gate so as to render the gate threshold voltage of selected transistors sufficiently high so that they will not turn on. The configuration of the selected transistors corresponds to the ROM program code.

The aforementioned ion implantation must be done at a sufficiently high energy to put the peak of the as-implanted profile under the oxide/channel interface, which means that the boron must get through the gate oxide, poly gate, and whatever films are, at that point, on top of the polysilicon. There are three reasons why the peak must get that far:

a. The as-implanted distribution drops off from its peak concentration so rapidly that an impracticably longer implantation time would be required to bring a far-side tail concentration up to the needed value.

b. It is undesirable, with the doses involved, to leave the majority of the dopant back in the gate oxide and/or poly.

c. Small variations in thicknesses of barrier films cause larger variations in concentration of the tail distribution than near the peak (center).

In post-poly programming, the wafers have patterned poly gates, a mask is used to open up selected transistors, and the high energy ion implantation is performed. In the subsequent process steps, the implanted boron sees high enough temperatures to effect nearly 100 percent substitution and lattice annealing, but these process steps add to the turn-around time.

Commonly-owned U.S. Patent No. 4,356,042 (Gedaly, 1982) and U.S. Patent Nos. 4,333,164 (Orikabe et al, 1982) and 4,208,727 (Redwine et al., 1980) are typical of the post-poly techniques.

In post-metal programming, the wafers have patterned metal interconnections, a mask is used to open up selected transistors, the metal-to-poly dielectric is etched back to a small thickness over these transistors, and the high-energy ion implantation is performed. The highest subsequent temperature seen by the wafer is 425° C, which is not enough to activate the boron beyond its expected 25 percent (or so) as-implemented substitutional percentage, and, in fact, may deactivate some of the already substituted boron. Consequently, the dose used is five to ten times higher than in the post-poly programming case, and results in a rather wide threshold range and high degree of unannealed damage. The advantage, of course, is that only a minimal amount of processing remains to be done after programming. The yield, however, is historically and understandably lower than in the post-poly case.

U.S. Patent No. 4,390,971 (Kuo, 1983) describes a typical post-metal programming technique. The ROM array is programmed by first depositing the post-metal-oxide or protective oxide layer 21 over the entire slice, then patterning it by a photoresist mask and etch sequence using a unique mask which defines the ROM code. An aperture 22 is defined over each cell 10 to be programmed as a "0", and each cell 10 to be a "1" is left covered. The slice is then subjected to a boron implant of about 180 Kev to a dosage of about 10^{13} ions per sq. cm. The energy level and dosage are dependent upon the thickness of the oxide layer 19 and the polysilicon gates 11, as well as the change in threshold desired. At this level, the ion implant penetrates the polycrystalline silicon gate 11 and gate oxide 19 to create an implanted region 23 in the channel area. This implant raises the threshold voltage above 5 V. Since the part operates on a supply voltage Vdd of 5 V., the full logic 1 level will not turn on the transistor. The transistors covered by the oxide 21 will not be implanted so will retain the usual threshold voltage of about 0.8 V. U.S. Patent No. 4,198,693 (Kuo, 1980) describes a similar process for a VMOS ROM. Somewhat less voltage is required when the metal over the gates has been removed, as discussed in U.S. Patent No. 4,342,100 (Kuo, 1982). Even less voltage may be required when the implant is performed prior to metalization (forming contacts and interconnects), as described in U.S. Patent Nos. 4,364,167 (Donley, 1982) and 4,295,209 (Donley, 1981).

In both post-poly and post-metal boron implant type late programming, the high-energy ion implantation can have yield degrading effects.

Disclosure of the Invention

Therefore, it is an object of this invention to provide an improved technique for ROM programming, late in the process, which requires less implant voltage than the above-described techniques.

According to the invention, transistors having lateral gaps between their source and drain and the gate are interconnected in a ROM to receive program code.

In one embodiment of the invention (Fig. 3), the gaps of selected transistors are subjected to a phosphorous implant to create lightly doped n-

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In one embodiment of the invention (Fig. 3), the gaps of selected transistors (42) are subjected to a phosphorous implant (44) to create lightly doped n- regions (26,28) connecting the source (18) and drain (20) to the gate (14), and function normally. The other transistors (40) do not receive the phosphorous implant, and thus have a higher threshold voltage.

In another embodiment of the invention (Fig. 2) all of the transistors receive the phosphorous implant to create the n- regions (26,28) connecting the source and drain to the gate, and the n- regions of selected transistors (32) are counter-doped with a boron implant (34) so as to raise their threshold voltages, while the other transistors (30) are not counter-doped and function normally.

In both embodiments, programming can occur late in the processing of the ROM.

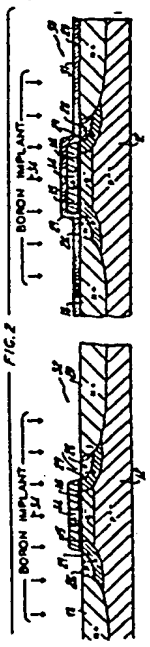

FIG. 2

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regions connecting the source and drain to the gate, and function normally. The other transistors do not receive the phosphorous implant, and thus have a higher threshold voltage.

In another embodiment of the invention (Fig. 2) all of the transistors receive the phosphorous implant to create the n- regions connecting the source and drain to the gate, and the n- regions of selected transistors are counter-doped with a boron implant so as to raise their threshold voltages, while the other transistors are not counter-doped and function normally.

In both embodiments, programming can occur late in the processing of the ROM.

Other objects, features, and advantages of the invention will become apparent in light of the following description thereof.

Brief Description of the Drawings

Fig. 1 is a cross-sectional view of a prior art transistor.

Fig. 2 is a cross-sectional view of one embodiment of the invention.

Fig. 3 is a cross-sectional view of another embodiment of the invention.

Best Mode for Carrying Out the Invention

Fig. 1 illustrates one FET device 10 of a large scale integrated circuit. The substrate 12 of the device is a silicon material lightly doped with a P-type material, such as boron, and designated as a P-- region. A gate 14 is separated from the silicon substrate 12 by a layer of silicon dioxide 15. A channel region 16 above the P-- region 12 and below the gate 14 is slightly more heavily doped with a P-type material than the substrate 12 and is designated as a P-region.

A source 18 and drain 20 are formed by heavily doping regions of the substrate 12 on opposite sides of the gate 14 with an N-type material and designated as an N+ region.

Lateral gaps exist between each of the source and drain and the gate. To connect the source and drain to the gate, the gaps are electrically closed by a blanket, low-dose phosphorous implant, resulting in n- gap regions 26 and 28 respectively. (Although the n- implant may extend over the source and drain, it is only the n- implant in the gaps that is germane to the invention, as described hereinafter). Additionally, boron-doped "halo" regions 29 are doped with P-type material in a greater concentration than the channel region, and extend around the n- gap regions 26 and 28 to improve short-channel characteristics and to support shallow punchthrough and V_T falloff.

The above-described process is described in greater detail in copending, commonly-owned U.S. Patent Application Serial No. 335,608, filed on December 30, 1981 by Y. P. Han and Chan and entitled TRIPLE DIFFUSED SHORT CHANNEL DEVICE STRUCTURE.

In one embodiment of the invention, as shown in Fig. 2, a transistor 30 is masked by a layer of photoresist 31, and a transistor 32 is not. (The transistors 30 and 32 are of the type shown in Fig. 1.) The substrate is then subjected to a low-energy, low-dose boron implant, as indicated by arrows 34. In the unmasked transistor 32, the n- regions 26 and 28 are compensated by the boron implant 34 so as to change said regions to P-type (as indicated), thereby resulting in an abnormally high threshold voltage in the transistor 32. The transistor 30 is shielded from the boron implant by the photoresist, which is later removed, so as to function in a normal manner. (The transistor 30 is identical to the transistor 10.) This sequence allows the program code to be installed very late in the processing sequence, in some cases even after metal interconnections are made.

The energy of the boron implant 34 is on the order of 50 to 75 Kev since it need only compensate the shallow n- gap regions 26 and 28. Furthermore, the dose of the boron implant may be low, on the order of 10^{14} ions per sq. cm., since the n- gap region is only lightly dosed with phosphorous initially. (The dose is conveniently low so that an overdose error would not result in the formation of a zener n+/p+ junction between the source and drain). A benefit of this embodiment is that the boron counter-implant increases the "halo" 29 doping which further negates short channel effects. A further benefit of this embodiment is that the boron counter-implant causes the P-type concentration at the upper surface of the "halo" region to be sufficiently high to prevent threshold instability due to charge accumulation at said surface.

In an alternate embodiment of the invention, as shown in Fig. 3, a transistor 40 is masked by a layer of photoresist 41 and a transistor 42 is not. (Except as described hereinafter, the transistors 40 and 42 are of the type shown in Fig. 1.) The photoresist mask is applied to selected transistors 40 prior to the aforementioned blanket, low-dose n- (phosphorous) implant, as indicated by the arrows 44. Therefore, the masked transistor 40 will not have the n- regions 26 and 28 connecting the source and drain to the gate, resulting in an extremely high threshold voltage. The unmasked transistor 42 receives the phosphorous implant which forms the connective n- gap regions 26 and 28 and functions in a normal manner. (The transistor 42 is identical to the transistor 10.)

Typically, in the embodiments of Fig. 2 and Fig. 3 the transistor having the normal threshold voltage (i.e., the transistors 30 and 42) would be indicative of logic ONE, and the transistor having the elevated threshold voltage (i.e., the transistors 32 and 40) would be indicative of logic ZERO in the program code.

It should be understood that various changes may be made to the invention without departing from the spirit and scope thereof.

Claims

1. A method of ROM manufacture comprising, the sequential steps of:

forming a plurality of transistors on a silicon

substrate (12), each transistor having a gate (14) formed on the substrate and a source (18) and a drain (20) formed in the substrate and spaced apart from the gate so as to create a lateral gap between the source and the gate and a lateral gap between the drain and the gate;
subjecting the substrate to a low-dose phosphorous implant so as to create n- gap regions (26,28) connecting the source and drain to the gate of each transistor;
masking selected transistors (30) according to a desired program code;
subjecting the substrate to a boron implant (34) so as to counter-dope the n- gap regions of the unmasked transistors;
wherein the masked transistors (30) have normal threshold voltages and the unmasked transistors (32) have greater than normal threshold voltages according to the desired program code.

2. A method according to claim 1 wherein the boron implant is performed at an energy of 50-75 Kev and at a dose of 10^{14} ions per sq. cm.

3. A method according to claim 1 wherein the boron implant changes the n- gap regions to P-type.

4. A method of ROM manufacture comprising, the sequential steps of:
forming a plurality of transistors on a silicon substrate (12), each transistor having a gate (14) formed on the substrate and a source (18) and a drain (20) formed in the substrate and spaced apart from the gate so as to create a lateral gap between the source and the gate and a lateral gap between the drain and the gate;
masking selected transistors (40) according to a desired program code;
subjecting the substrate to a low-dose phosphorous implant (44) so as to create n- gap regions (26,28) connecting the source and drain to the gate in the unmasked transistors;
wherein the unmasked transistors (42) have normal threshold voltages and the masked transistors (40) have greater than normal threshold voltages according to a desired program code.

FIG. 1

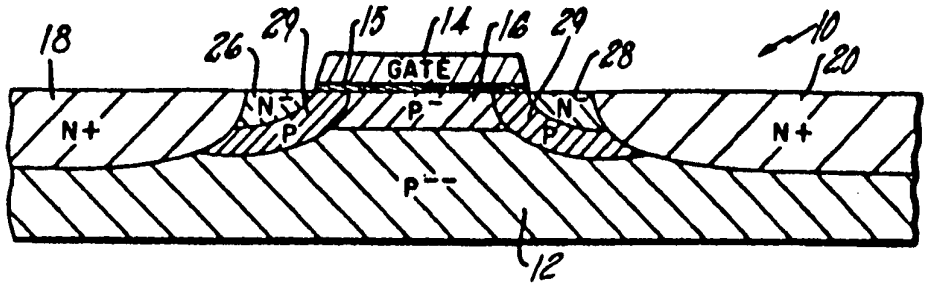

FIG. 2

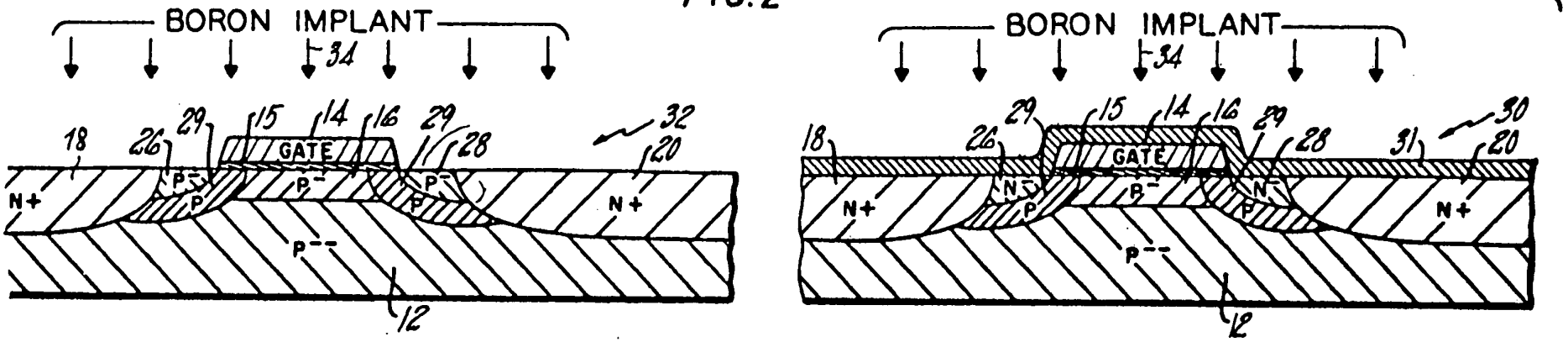

FIG. 3